IN THE DRAWINGS

Applicant acknowledges that the drawings filed on September 22, 2003, are accepted.

REMARKS

Claim 4 has been cancelled, claim 29 has been added, and claims 1, 3, 5-10, 12, 17, 19, 22-24, and 28 have been amended. Claims 1-3 and 5-29 are pending in the application.

In paragraph 3 of the Office Action, the Examiner asks to update the status of related US patent application referred to on page 1. There is no such reference to any related patent application in the present application. The Examiner is requested to clarify this request.

In the present Office Action, the Examiner objects to claims 4, 12, 16, 19, 24 and 28 due to informalities, arguing that the term "substantially" should be deleted for clarity. The Applicants agree with the Examiner's recommendation, in part because the use of the word "contemporaneously" in the claims obviates the need for the word "substantially." In the context of these claims, the term "contemporaneously" itself connotes that the burst length and latency information need not necessarily be provided at the exact time as the "command" to access the memory; instead, the use of this term connotes that the information and the command may be provided during the same time "period" (i.e., during a given time interval). In view of the foregoing, the term "substantially" has been deleted, as recommended by the Examiner.

Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Raynham*** (U.S. Patent No. 6,418,068). The Applicant traverses the rejection for the reasons presented below.

The present patent application explains prior art memory systems were capable of supporting multiple modes of operation (*i.e.*, different latency levels and/or burst lengths). Patent

Application, page 3, lines 16-21. The problem with these prior art systems, however, is that the operation mode of the memory device can only be altered by reprogramming its mode register. *Id.* The patent application describes that changing the operation mode of the memory device may be a time consuming process, as the reprogramming must be loaded (or reloaded) when all memory banks are idle and no bursts are in progress. *Id.*

The reference, ***Raynham***, cited by the Examiner effectively teaches what the Applicants describe in the background patent application. In particular, this reference describes the use of mode registers 316 (see Figure 1), which include latency and burst length information (see Figure 6). ***Raynham*** explains that these mode registers 316 have to be programmed each time a change to latency and burst length is desired. See ***Raynham***, 10:24-26 (explaining that once the register 316 have been programmed, it "retains the stored information until it is programmed again" or there is power lose).

To reduce the effect(s) of the shortcomings of the prior art, the present invention describes various embodiments for efficiently accessing memory. In general, in accordance with one or more embodiments of the present invention, the specification describes that the memory controller 160 is adapted to access the memory array module 150 at the **desired** burst length, the read (CAS) latency level, and/or write latency level based on the nature of the memory request received. For example, depending on the amount of data requested by the access device 120, the memory controller 160 selects the burst length and/or latency accordingly to accessing the desired data from the memory array module 150. In particular, if large amounts of data are desired by, for example, the main client 135 of the access device 120, the memory controller 160

may increase the burst length (and/or decrease the CAS latency level) associated with that memory access. Similarly, the burst length may be reduced (or the CAS latency level may be increased) for smaller data transfers, such as those requested by the peripheral client 140 of the access device 120.

Against this general backdrop, the claims of the present application are discussed. Consider claim 1, which, among other things, calls for determining the desired burst length information or latency information based on the nature of the received memory request. ***Raynham*** fails to teach at least this claimed feature. As explained and shown in Figure 6 of ***Raynham***, the burst length and latency information is programmed into the mode register 316. Further, as ***Raynham*** explains, once this register is set, the latency and burst length remains fixed until that register is reprogrammed again. ***Raynham***, 10:24-28. Thus, in ***Raynham***, once the Mode register 316 has been programmed, the same latency/burst length values defined in the mode register 316 are used for any and all incoming memory requests (regardless of the nature of that request). As such, the latency/burst length values in ***Raynham*** are not determined based on the nature of the received memory request. In contrast, claim 1 calls for determining the latency and/or burst length information "based" on the received memory request. For example, as described in the Specification, the latency/burst length information may be determined "based" on the amount of data being read or written in connection with a memory access. In alternative embodiments, the burst length/latency information may be determined "based" on other suitable criteria.

For at least the foregoing reason, claim 1 and its dependent claims are allowable. Moreover, the other claims are also allowable for the features recited therein. For example, claim 10 calls for a controller adapted to determine at least one of burst length information and latency information based on the nature of the memory request received from the source. Because ***Raynham*** does not teach at least this claimed feature, claim 10 and its dependent claims are allowable. Similarly, other claims are allowable in view of the features recited therein.

The newly added claim 29 is allowable because the cited reference at least does not teach a controller that is adapted to access the memory using different burst lengths without requiring reprogramming of a register holding information relating to burst length.

The Applicant clarifies that the pending claims do not exclude the use of the mode registers. To the contrary, the claims expressly allow for such a possibility. The claims do, however, call for determining the latency or burst length value based on the received memory request. The latency/burst length values may be stored in a mode register (or any other storage location), where the appropriate value is then determined (or selected) based on received memory request.

The Examiner is invited to contact the undersigned attorney at (713) 934-4064 with any questions, comments or suggestions relating to the referenced patent application.

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